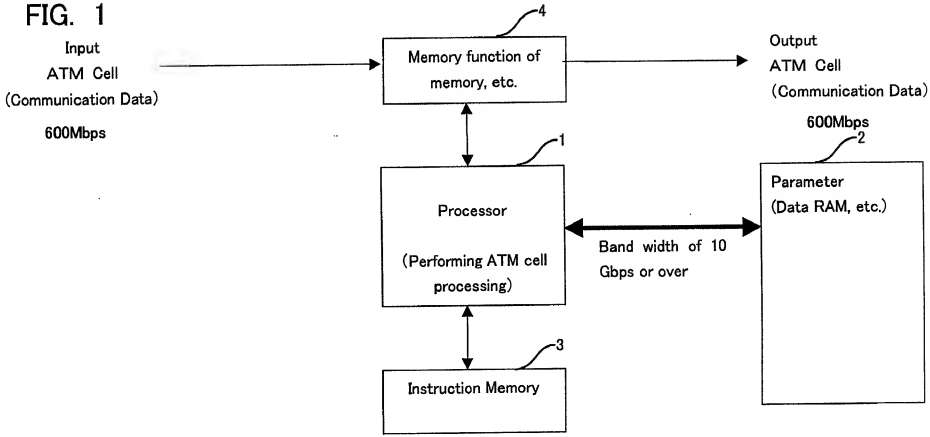
FIG. 1


Input
ATM Cell
(Communication Data)
600Mbps
4
Memory function of memory, etc.
Output
ATM Cell
(Communication Data)
600Mbps
1
Processor
(Performing ATM cell processing)
Band width of 10 Gbps or over
2
Parameter
(Data RAM, etc.)
3
Instruction Memory

JP 2020-087260

FIG. 2

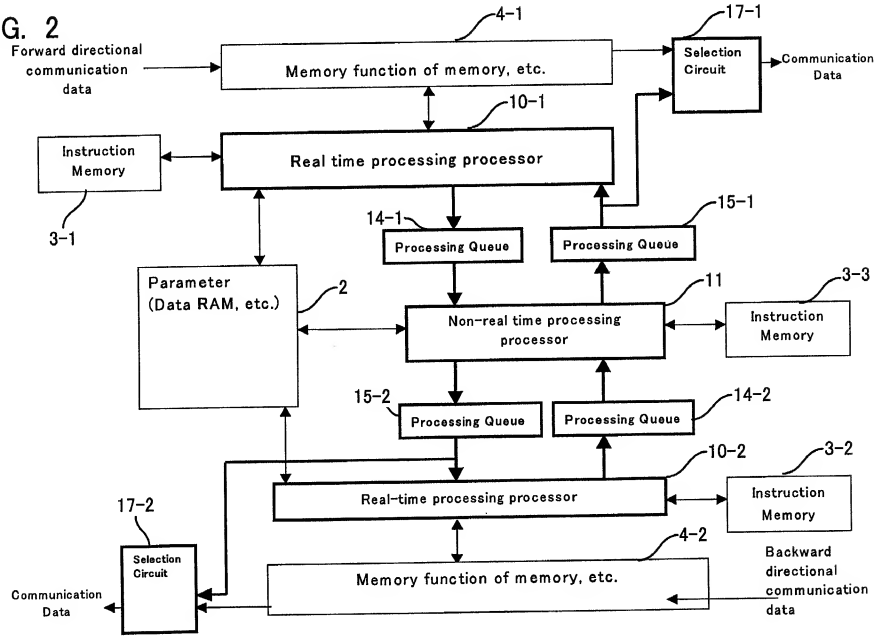


FIG. 3

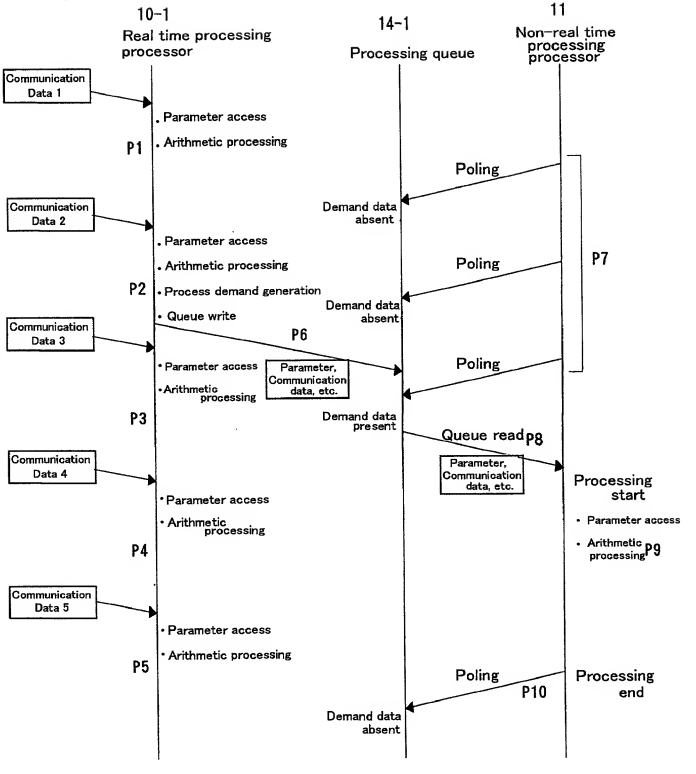

10-1
Real time processing processor
14-1
Processing queue
11
Non-real time processing processor
Communication Data 1
• Parameter access
• Arithmetic processing
P1
Poling
Demand data absent
Communication Data 2
• Parameter access
• Arithmetic processing
Poling
P7
P2
• Process demand generation
Demand data absent
Communication Data 3
• Queue write
P6
• Parameter access
• Arithmetic processing
Parameter, Communication data, etc.
Poling
P3
Demand data present
Queue read P8
Parameter, Communication data, etc.
Communication Data 4
Processing start
• Parameter access
• Arithmetic processing
P4
• Parameter access
• Arithmetic processing P9
Communication Data 5
• Parameter access
• Arithmetic processing
P5
Poling
Processing end
P10
Demand data absent

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FIG. 4

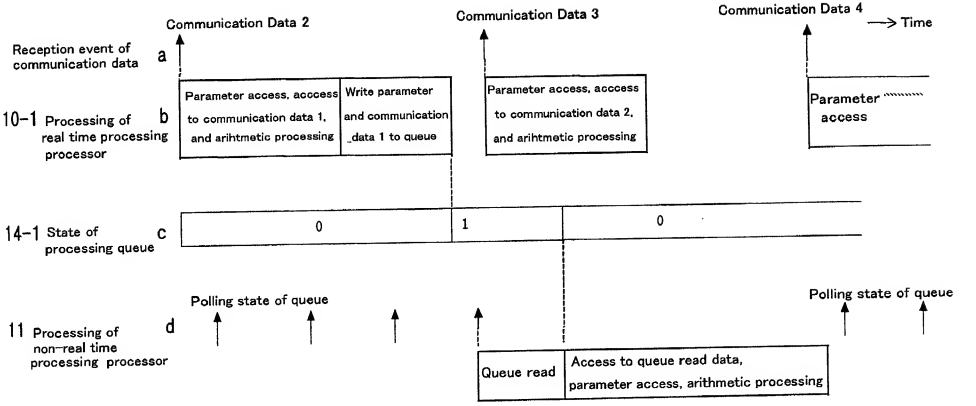
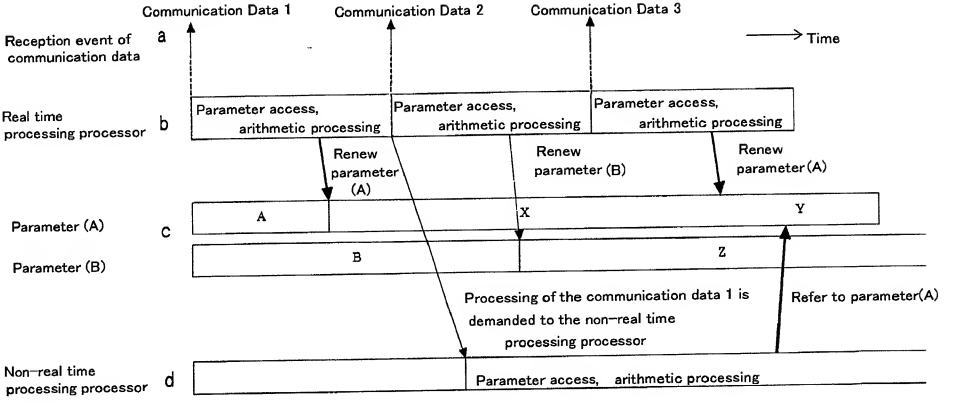
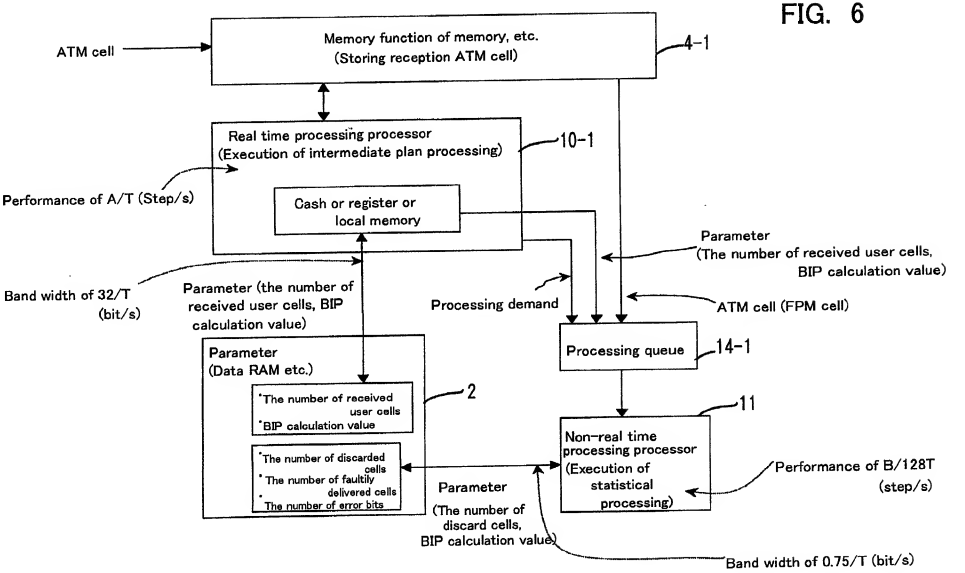


FIG. 5


Communication Data 1
Communication Data 2
Communication Data 3
Reception event of communication data
a
Time
Real time processing processor
b
Parameter access, arithmetic processing
Parameter access, arithmetic processing
Parameter access, arithmetic processing
Renew parameter (A)
Renew parameter (B)
Renew parameter (A)
Parameter (A)
c
A
X
Y
Parameter (B)
B
Z
Processing of the communication data 1 is demanded to the non-real time processing processor
Refer to parameter(A)
Non-real time processing processor
d
Parameter access, arithmetic processing

JP 2001-257680

FIG. 6



JP 2000-078160

FIG. 7

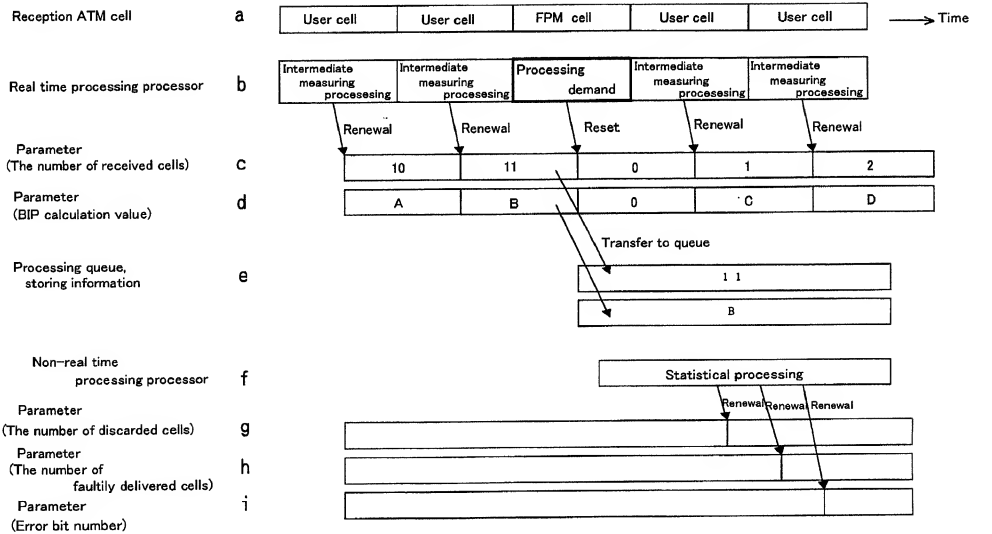


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FIG. 8A

ATM cell transmission side

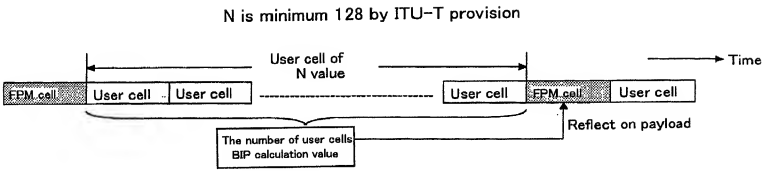



FIG. 8B

ATM cell reception side

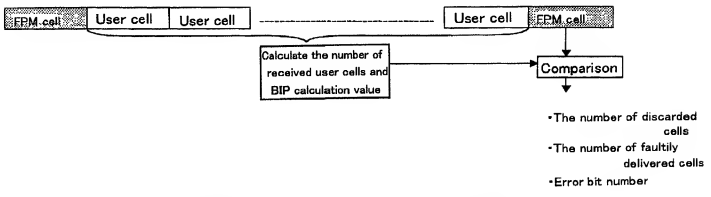



FIG. 8C

ATM cell flow

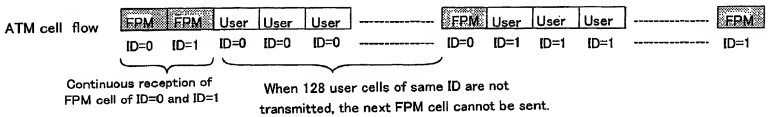


FIG. 9

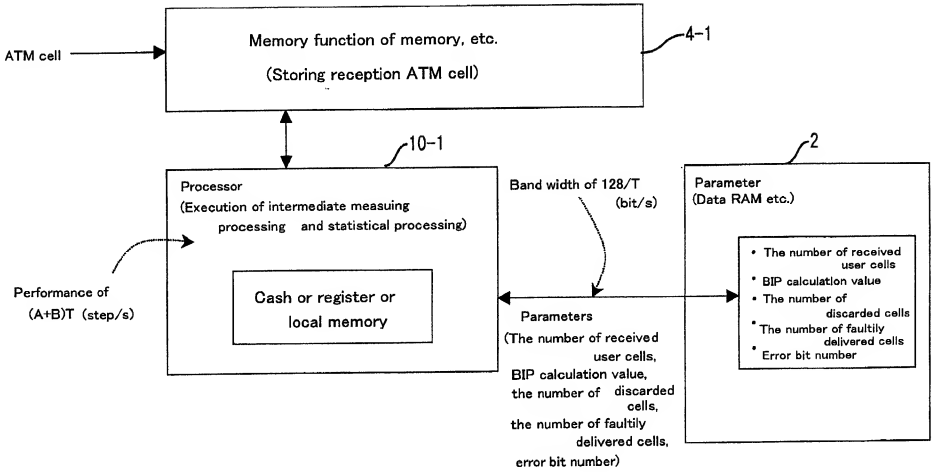

ATM cell
Memory function of memory, etc.
(Storing reception ATM cell)
4-1
10-1
Processor
(Execution of intermediate measuing processing and statistical processing)
Cash or register or local memory
Performance of (A+B)T (step/s)
Band width of 128/T (bit/s)
Parameters
(The number of received user cells, BIP calculation value, the number of discarded cells, the number of faultily delivered cells, error bit number)
2
Parameter
(Data RAM etc.)
• The number of received user cells
• BIP calculation value
• The number of discarded cells
• The number of faultily delivered cells
• Error bit number

FIG. 10

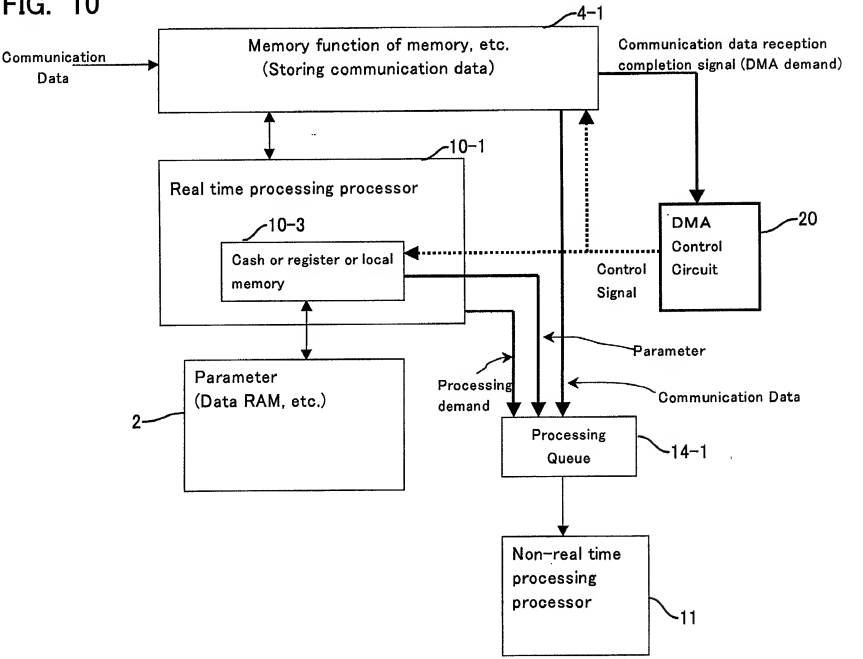

4-1
Memory function of memory, etc.
(Storing communication data)
Communication
Data
Communication data reception
completion signal (DMA demand)
10-1
Real time processing processor
10-3
Cash or register or local
memory
DMA
Control
Circuit
20
Control
Signal
Parameter
Parameter
(Data RAM, etc.)
2
Processing
demand
Communication Data
Processing
Queue
14-1
Non-real time
processing
processor
11

FIG. 11

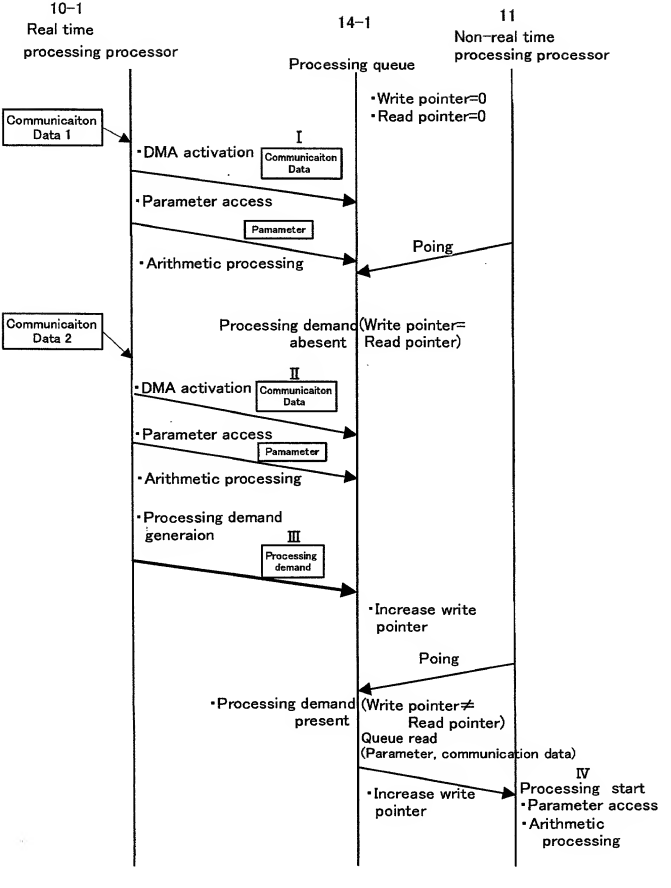
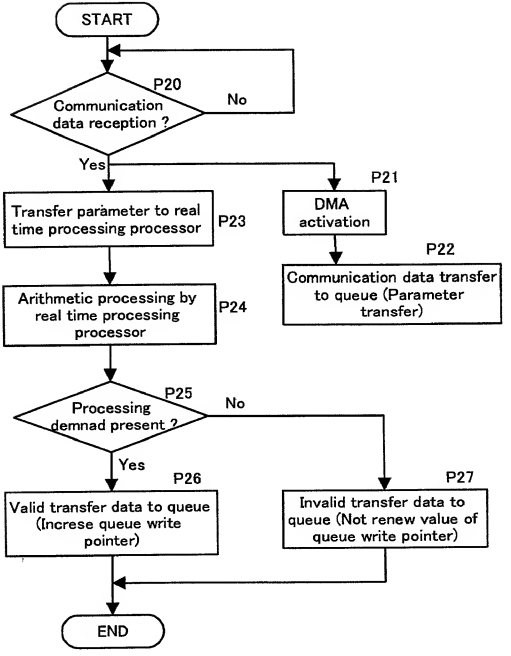

10-1
Real time processing processor
14-1
Processing queue
11
Non-real time processing processor
Communicaiton Data 1
・DMA activation
I
Communicaiton Data
・Write pointer=0
・Read pointer=0
・Parameter access
Pamameter
Poing
・Arithmetic processing
Communicaiton Data 2
Processing demand absent
(Write pointer= Read pointer)
・DMA activation
II
Communicaiton Data
・Parameter access
Pamameter
・Arithmetic processing
・Processing demand generaion
III
Processing demand
・Increase write pointer
Poing
・Processing demand present
(Write pointer≠ Read pointer)
Queue read
(Parameter, communication data)
IV
・Increase write pointer
Processing start
・Parameter access
・Arithmetic processing

FIG. 12


START
P20
Communication data reception ?
No
Yes
P21
DMA activation
Transfer parameter to real time processing processor
P23
P22
Communication data transfer to queue (Parameter transfer)
Arithmetic processing by real time processing processor
P24
P25
Processing demnad present ?
No
Yes
P26
Valid transfer data to queue (Increse queue write pointer)
P27
Invalid transfer data to queue (Not renew value of queue write pointer)
END

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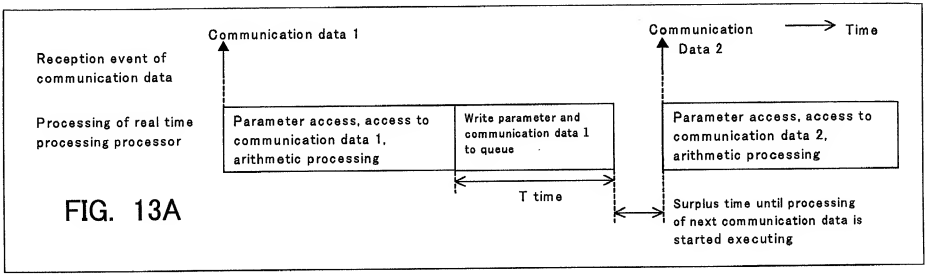


FIG. 13A

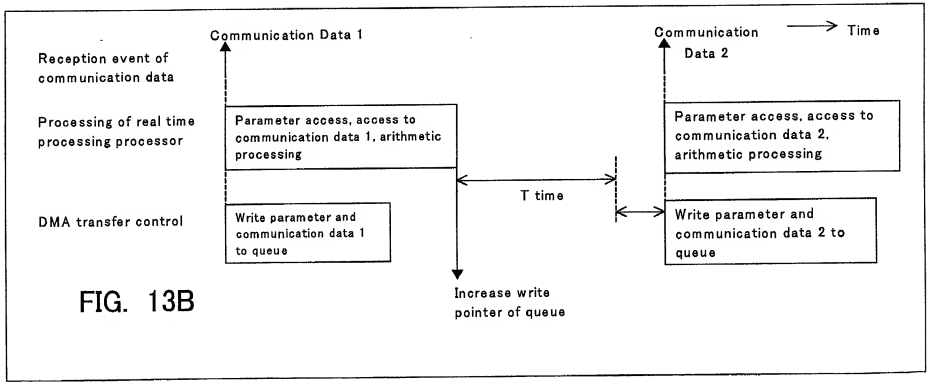


FIG. 13B

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FIG. 14

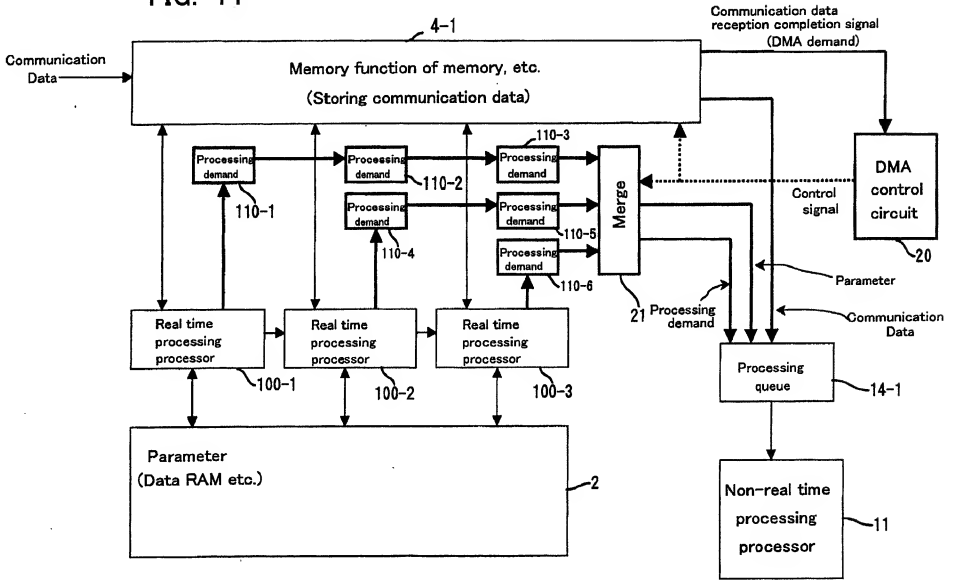

FIG. 15

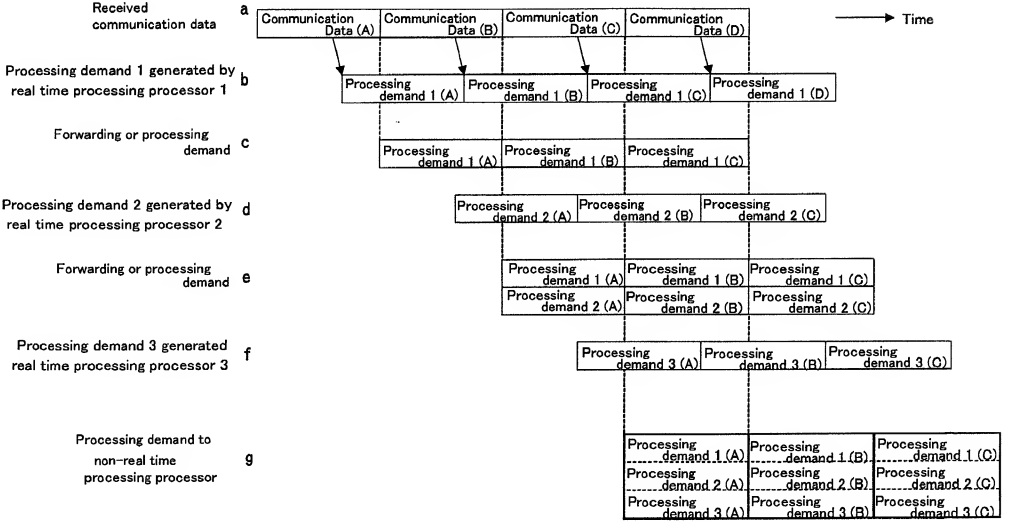
Received communication data
a
Communication Data (A)
Communication Data (B)
Communication Data (C)
Communication Data (D)
Time
Processing demand 1 generated by real time processing processor 1
b
Processing demand 1 (A)
Processing demand 1 (B)
Processing demand 1 (C)
Processing demand 1 (D)
Forwarding or processing demand
c
Processing demand 1 (A)
Processing demand 1 (B)
Processing demand 1 (C)
Processing demand 2 generated by real time processing processor 2
d
Processing demand 2 (A)
Processing demand 2 (B)
Processing demand 2 (C)
Forwarding or processing demand
e
Processing demand 1 (A)
Processing demand 1 (B)
Processing demand 1 (C)
Processing demand 2 (A)
Processing demand 2 (B)
Processing demand 2 (C)
Processing demand 3 generated real time processing processor 3
f
Processing demand 3 (A)
Processing demand 3 (B)
Processing demand 3 (C)
Processing demand to non-real time processing processor
g
Processing demand 1 (A)
Processing demand 1 (B)
Processing demand 1 (C)
Processing demand 2 (A)
Processing demand 2 (B)
Processing demand 2 (C)
Processing demand 3 (A)
Processing demand 3 (B)
Processing demand 3 (C)

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FIG. 16

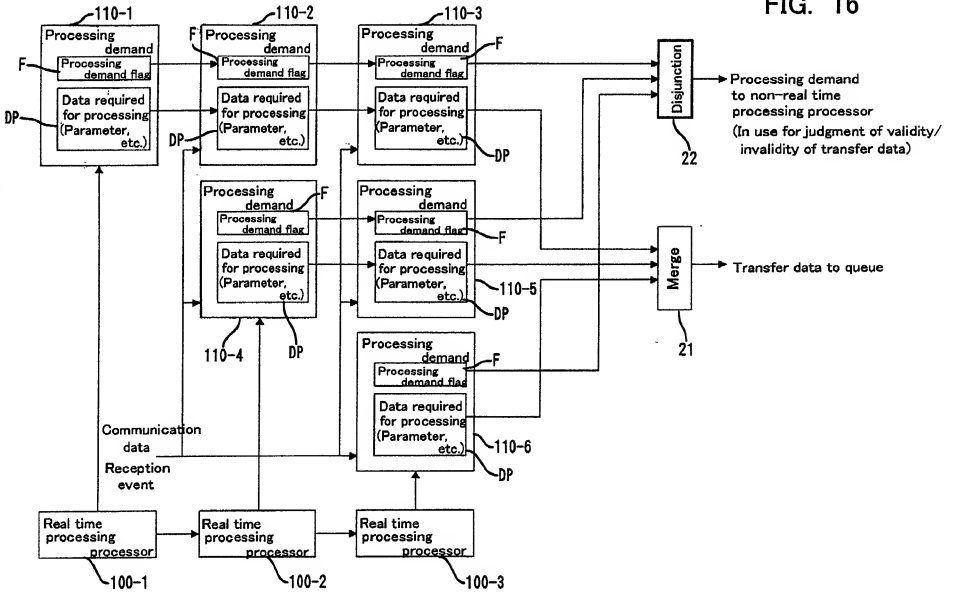

FIG. 17

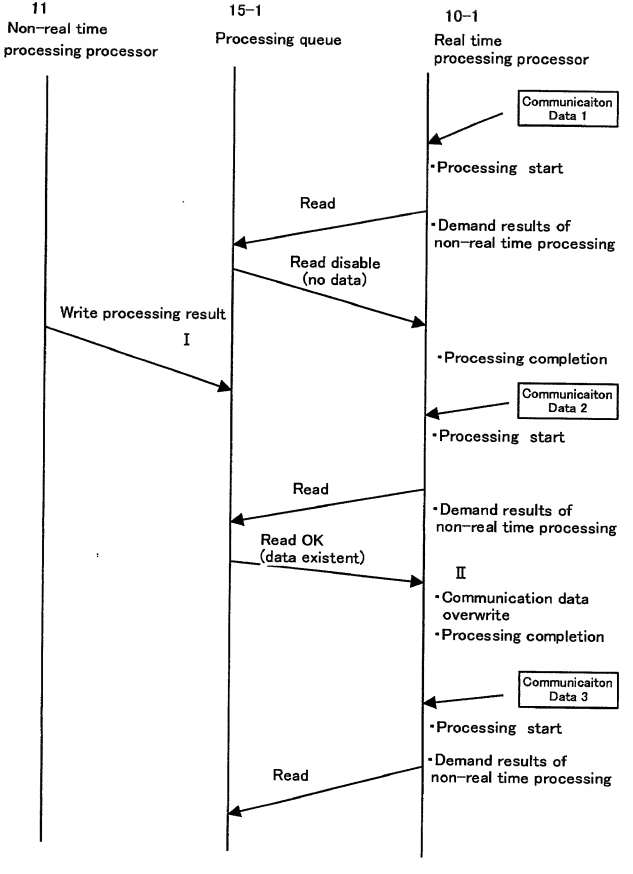
11
Non-real time processing processor
15-1
Processing queue
10-1
Real time processing processor
Communicaiton Data 1
•Processing start
Read
•Demand results of non-real time processing
Read disable (no data)
Write processing result
I
•Processing completion
Communicaiton Data 2
•Processing start
Read
•Demand results of non-real time processing
Read OK (data existent)
II
•Communication data overwrite
•Processing completion
Communicaiton Data 3
•Processing start
•Demand results of non-real time processing
Read

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FIG. 18

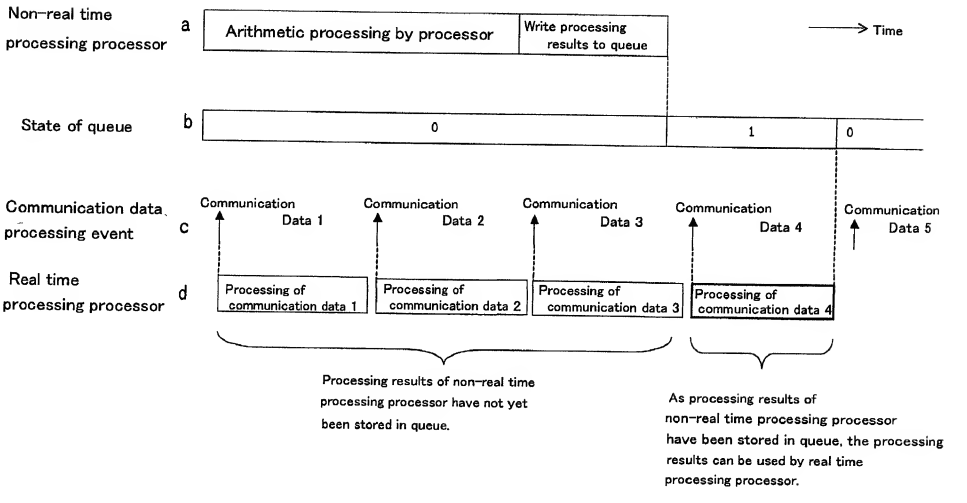
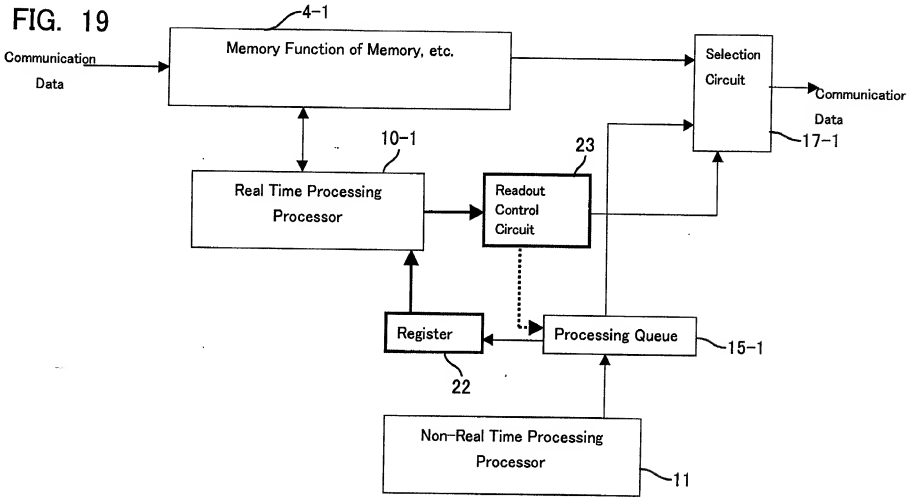


FIG. 19


4-1
Memory Function of Memory, etc.
Communication Data
Selection Circuit
Communication Data
17-1
10-1
Real Time Processing Processor
23
Readout Control Circuit
Register
22
Processing Queue
15-1
Non-Real Time Processing Processor
11